International Test Conference 2022

Industry Evaluation of Reversible Scan Chain Diagnosis

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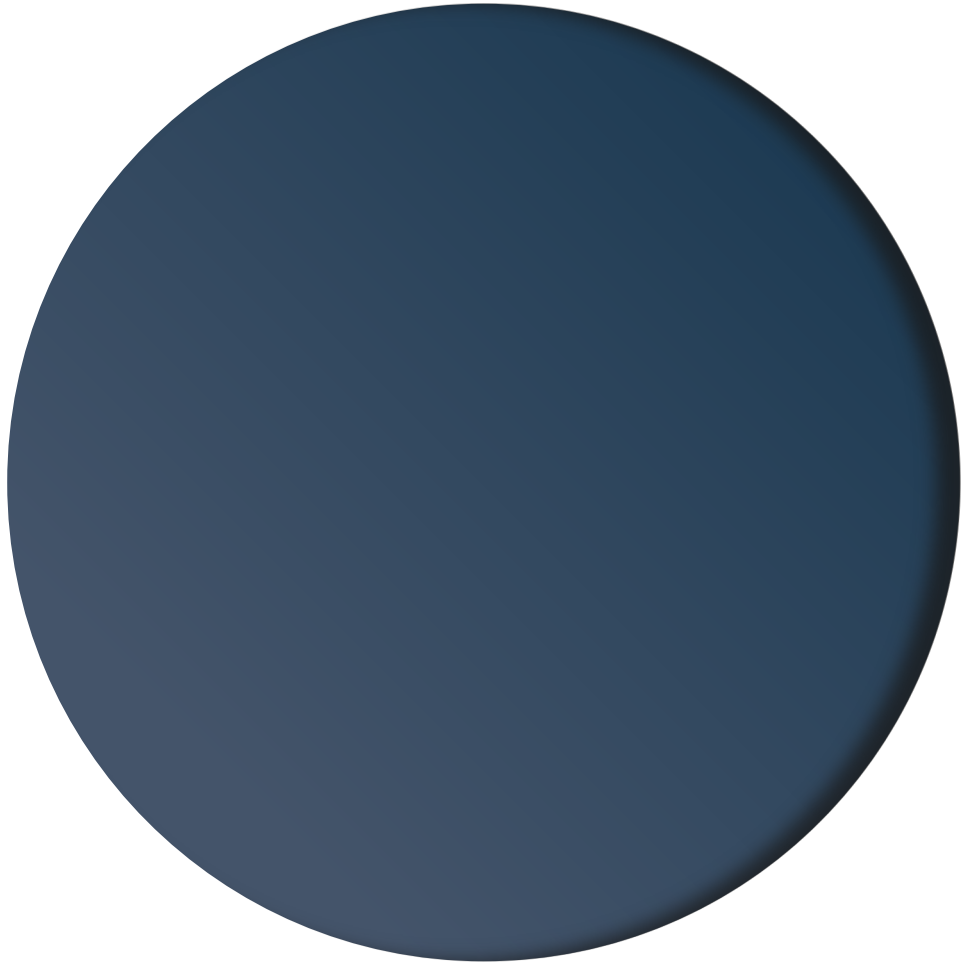
SIEMENS

Outline

- Scan Chain Diagnosis: Motivation and Background
- Reversible Scan Chain: Architecture, Operation
- Reversible Scan Chain: Diagnosis
- Silicon Evaluation
- Failure Analysis
- Conclusion

Scan Chain Diagnosis Introduction

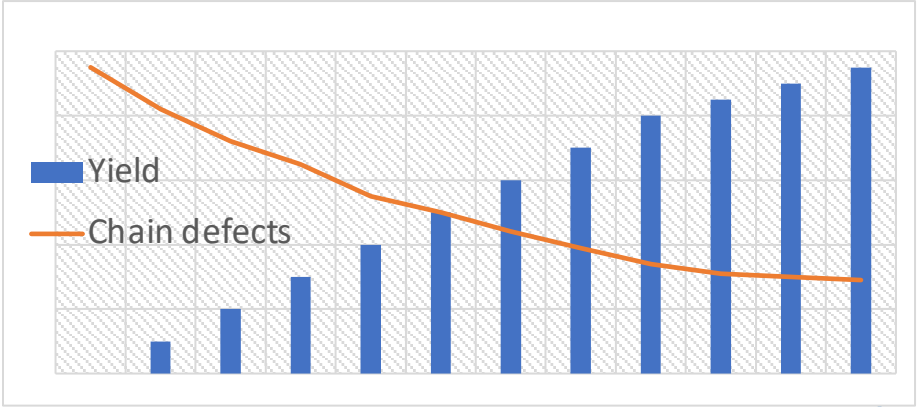


Scan Chain Diagnosis: Motivation

- Every new process node brings
  - Increasing chip density and complexity
  - Creative transistor structures
  - New design and manufacturing challenges
  - Unfamiliar defect behaviors
- Need to continuously improve scan diagnosis

- FA and time-to-yield challenges
- Diminishing time-to-market requirements

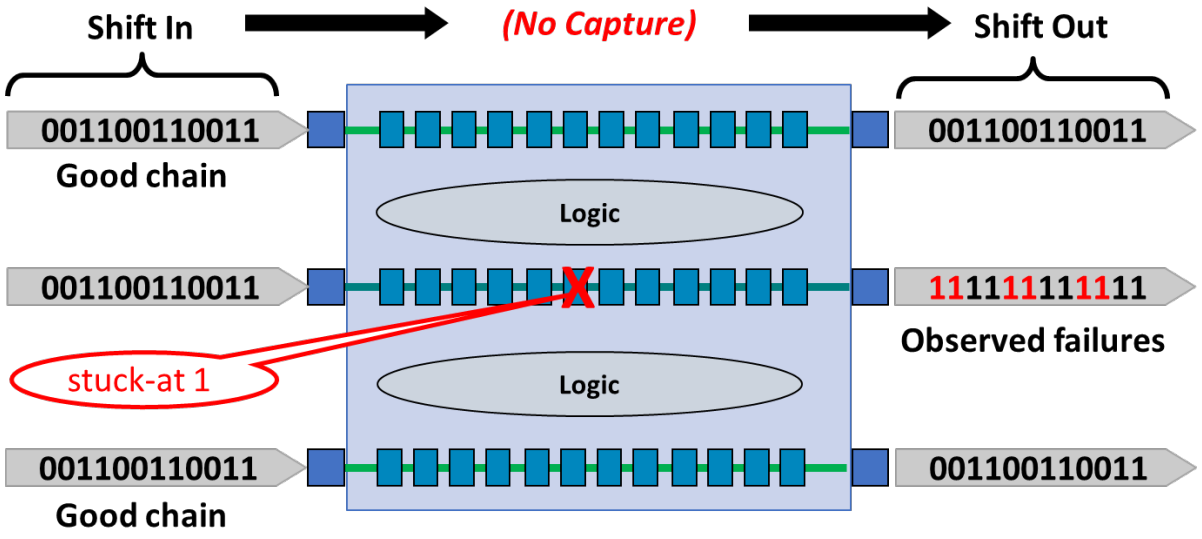
- Chain fail rate typically higher in node qualification/test chips and NPI
- Chain diagnosis crucial for rapid yield learning

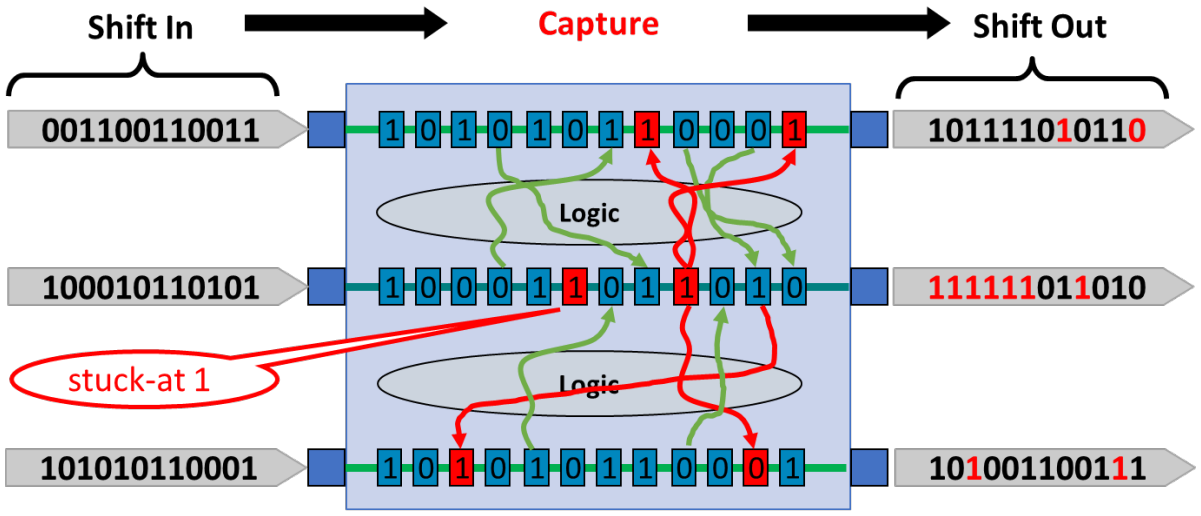


Scan Chain Diagnosis: Background

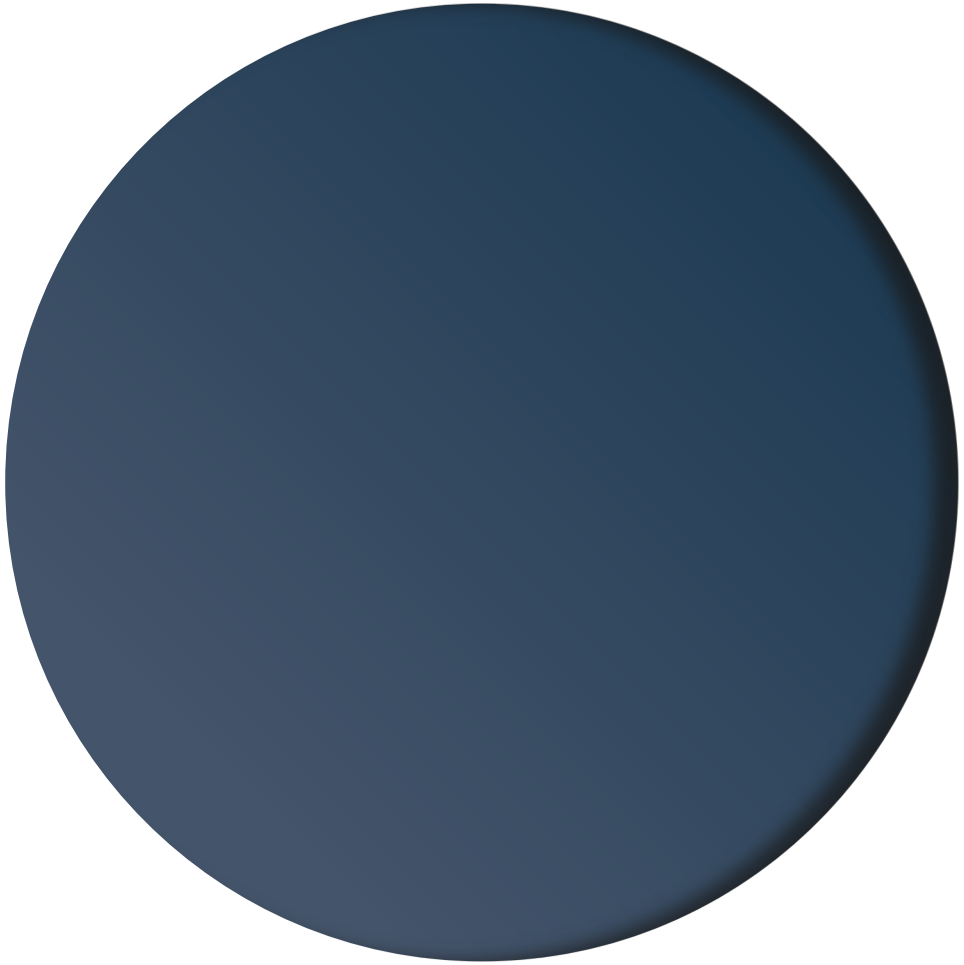
Conventional scan chain diagnosis uses

- Flush (chain) patterns to identify the defective chain and behavior
- Capture (scan) patterns to identify the defective scan cell



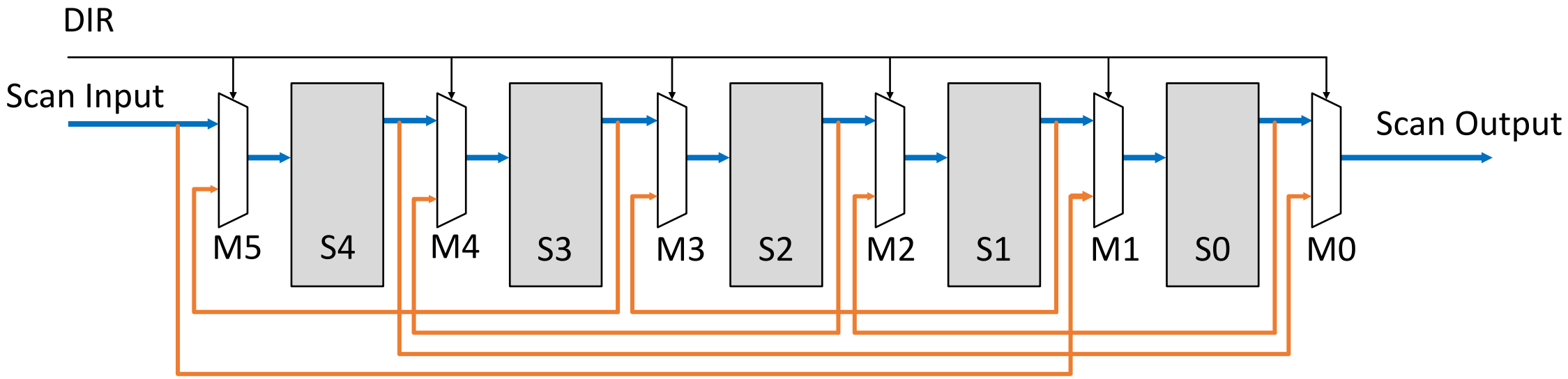


Reversible Scan Chain Architecture and Operation



Reversible Scan Chain Architecture

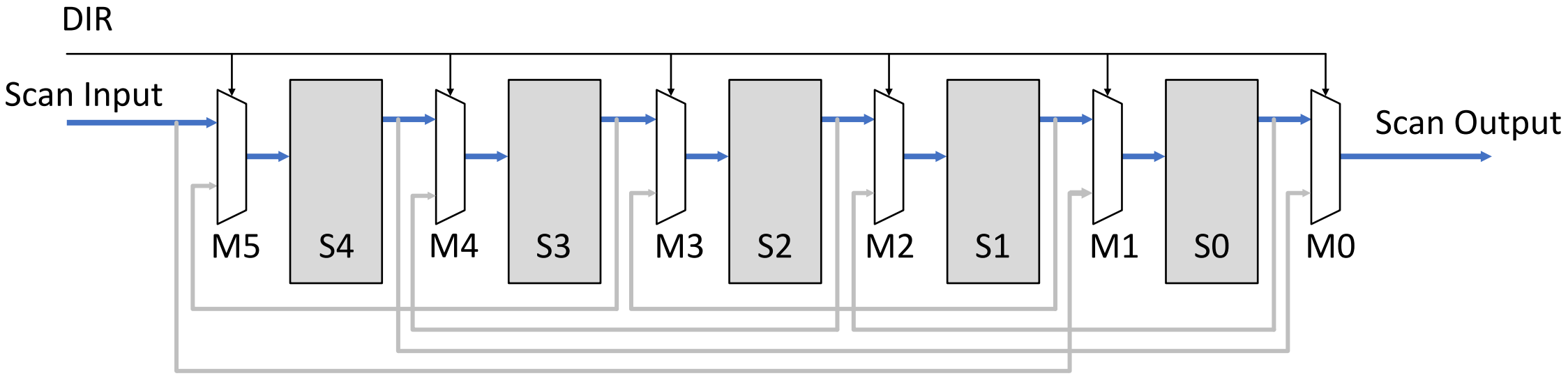
- Conventional scan chain – shifts data in a single direction
- Reversible scan chain – shifts data in two directions
- Each scan cell can receive shift values from its left or right neighbor
- Shift direction is controlled by a control pin (DIR)



Forward (conventional) shift direction
Reverse shift direction

Reversible Scan Chain Operation

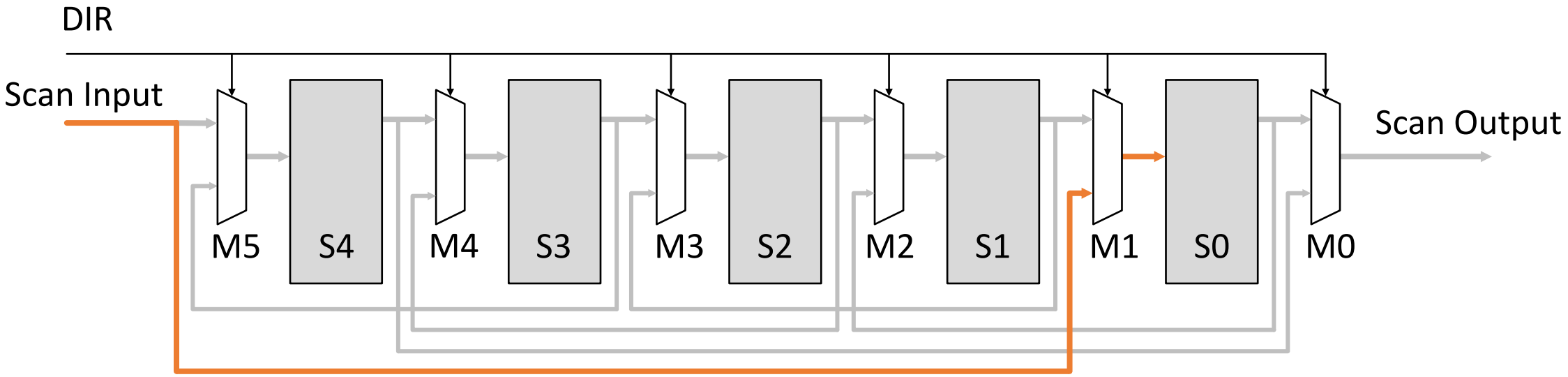
Left to Right (L2R) shift operation - DIR pin is asserted (DIR = 1)



Scan Input ➔ S4 ➔ S3 ➔ S2 ➔ S1 ➔ S0 ➔ Scan Output

Reversible Scan Chain Operation

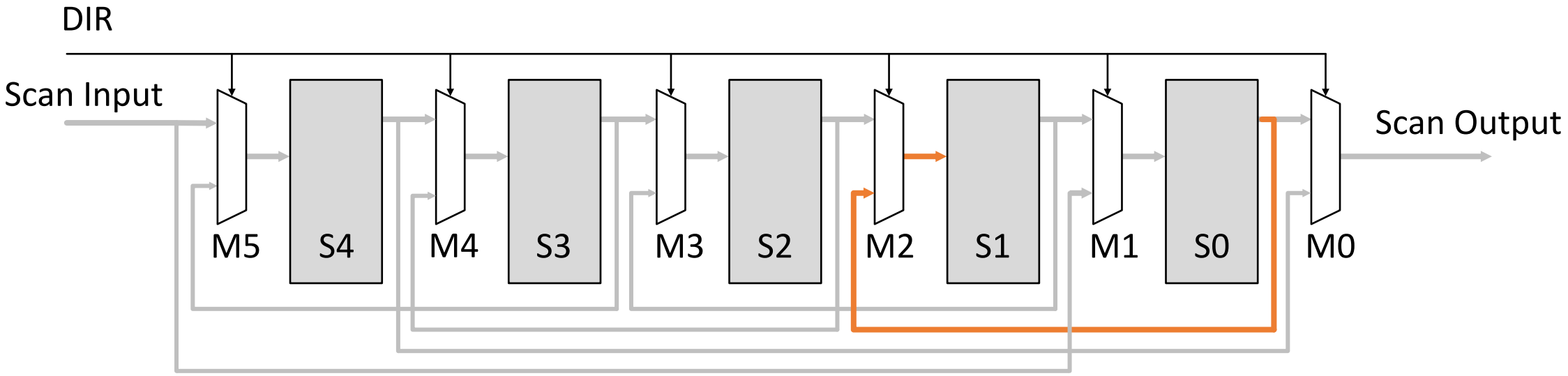
Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

Reversible Scan Chain Operation

Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

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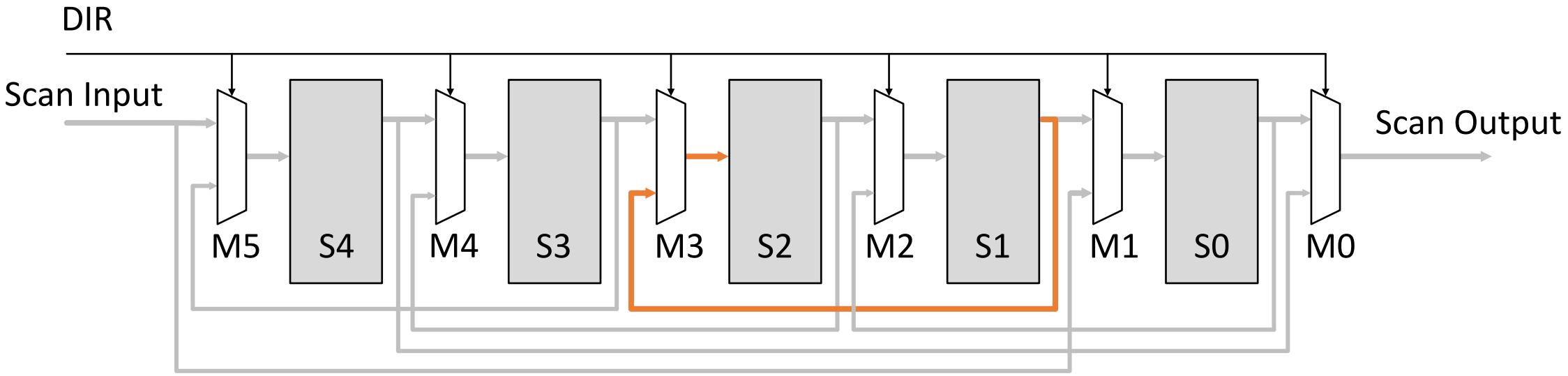
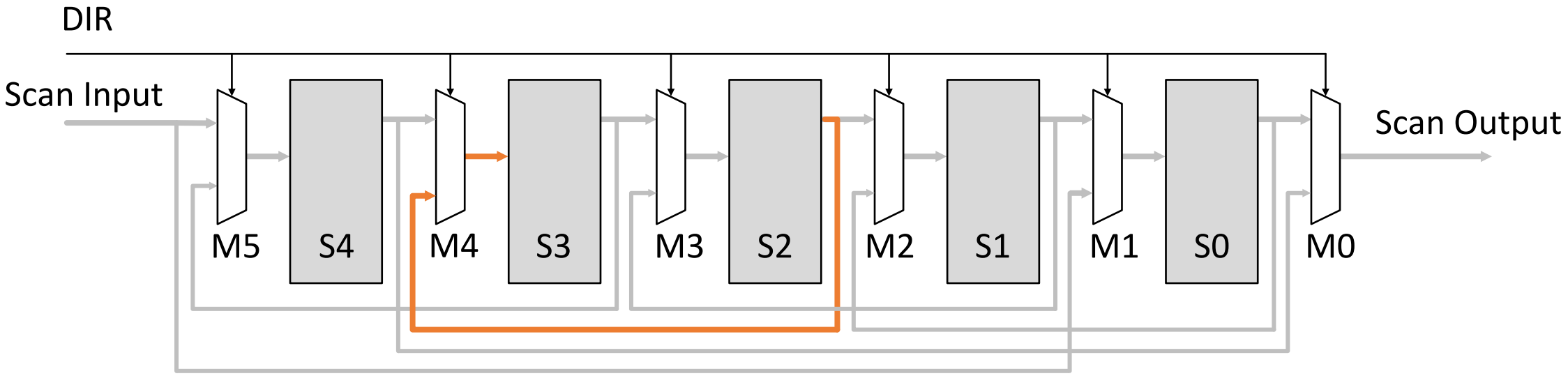
Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

Reversible Scan Chain Operation

Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

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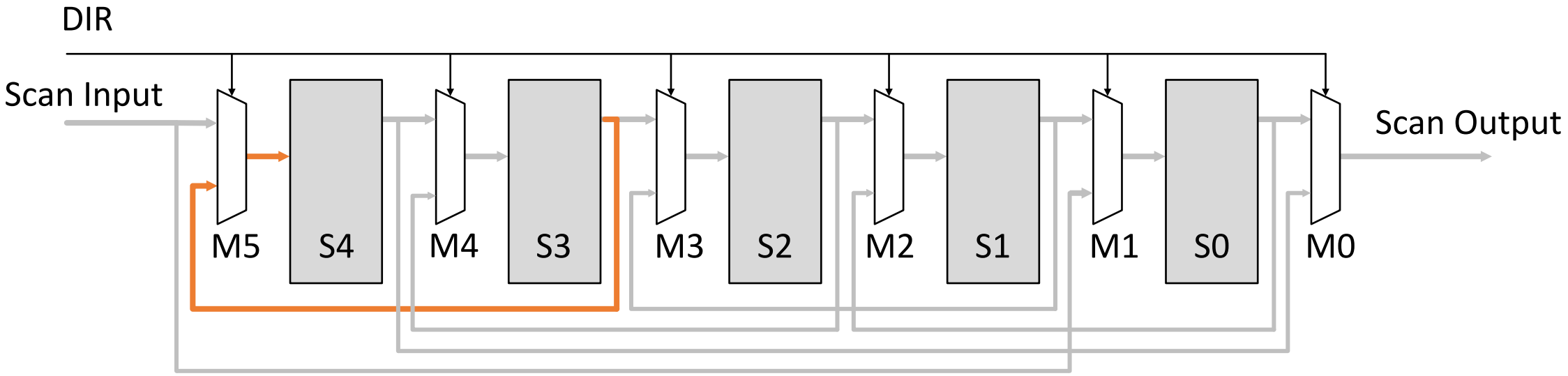
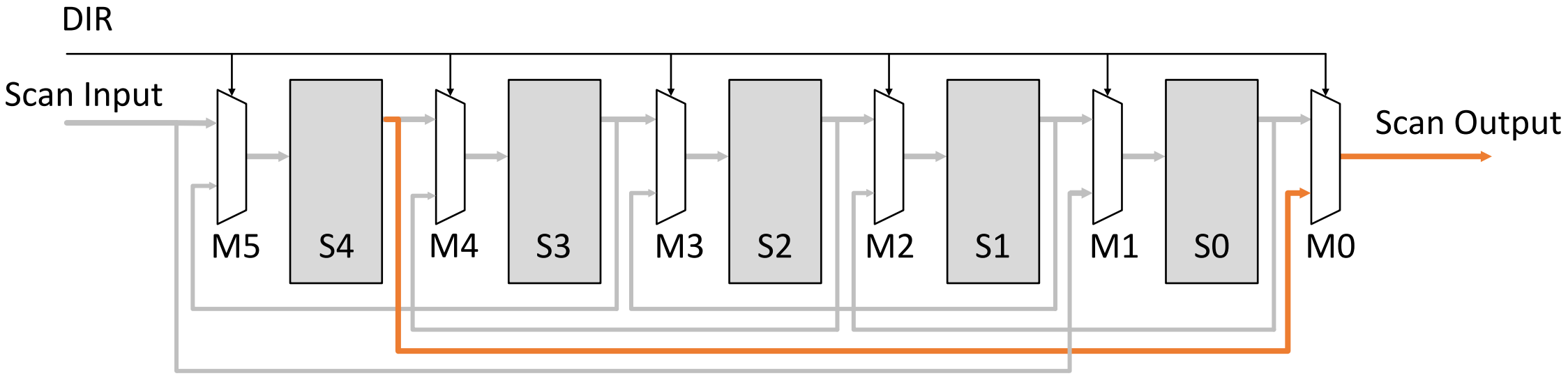
Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

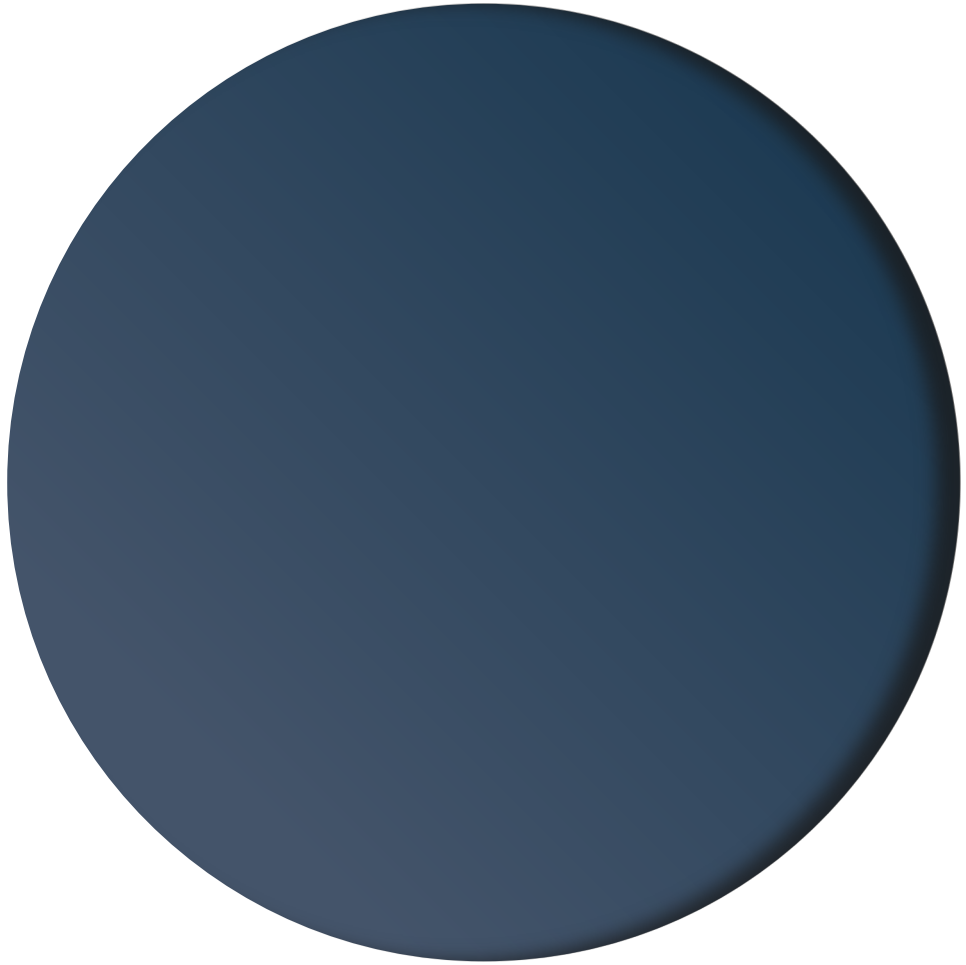
Reversible Scan Chain Operation

Right to Left (R2L) shift operation - DIR pin is de-asserted (DIR = 0)



Scan Input → S0 → S1 → S2 → S3 → S4 → Scan Output

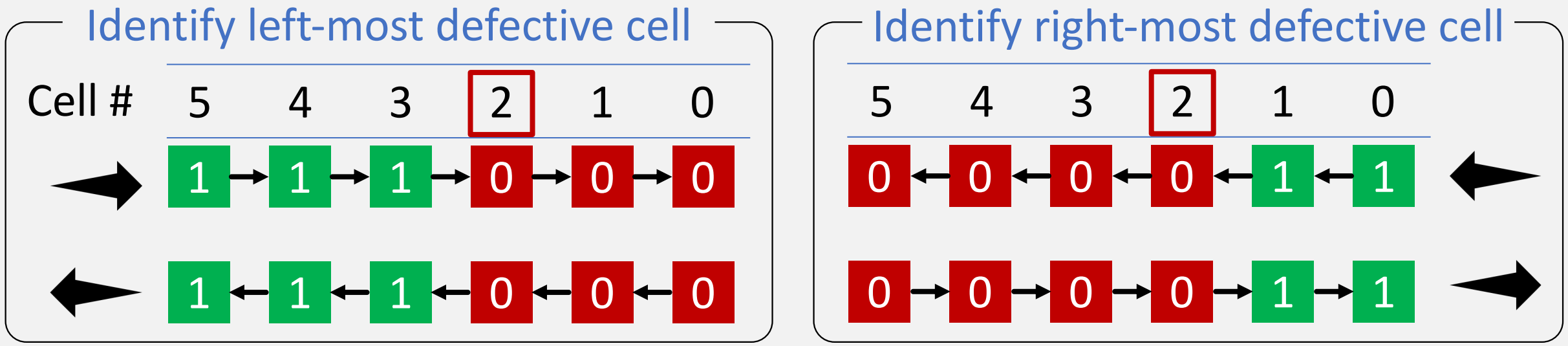
Reversible Scan Chain Diagnosis



Reversible Scan Chain Diagnosis

- Conventional scan chain diagnosis – Both flush and capture patterns needed
- Reversible scan chain diagnosis – Only flush patterns needed

Example 1: Stuck-at 0 fault in cell position 2

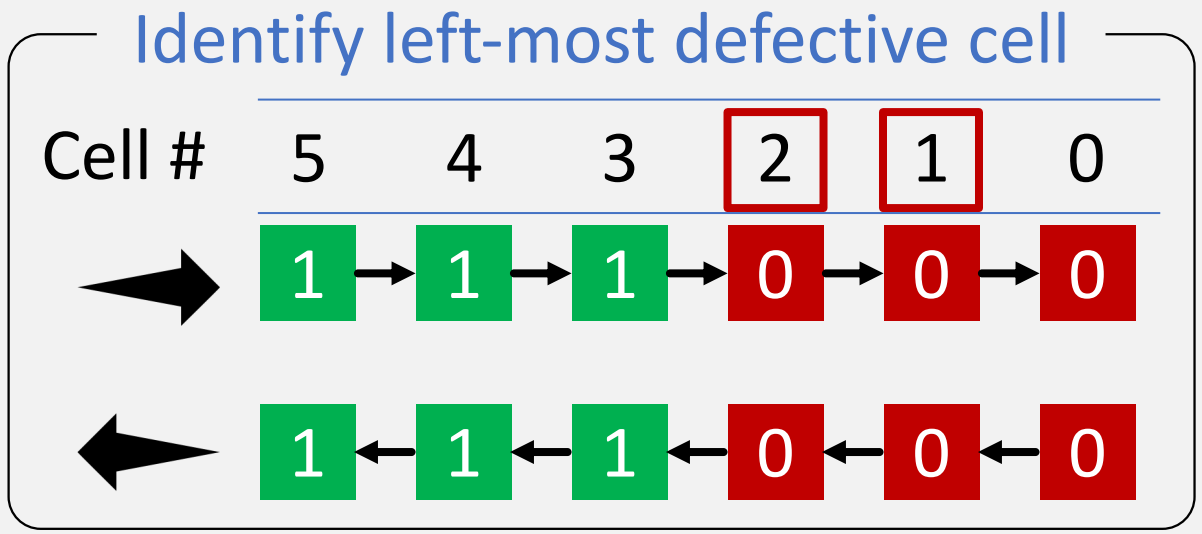


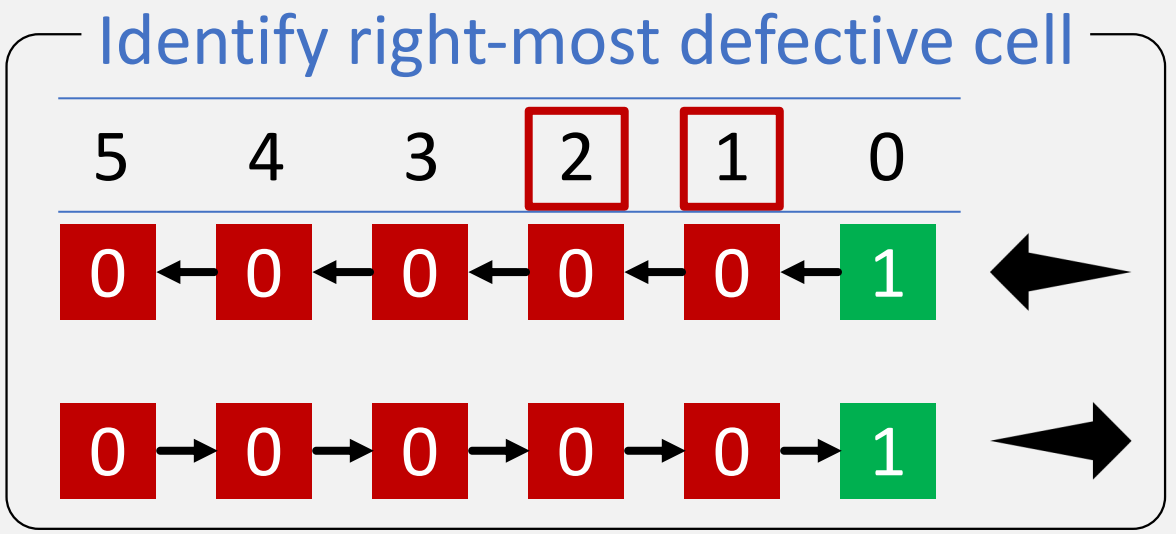
1. Load pattern from L2R: 111111
2. Unload pattern from R2L: 111000
3. Load pattern from R2L: 111111
4. Unload pattern from L2R: 000011

Reversible Scan Chain Diagnosis

- Conventional scan chain diagnosis – Both flush and capture patterns needed
- Reversible scan chain diagnosis – Only flush patterns needed

Example 2: Stuck-at 0 faults in cell positions 1 and 2



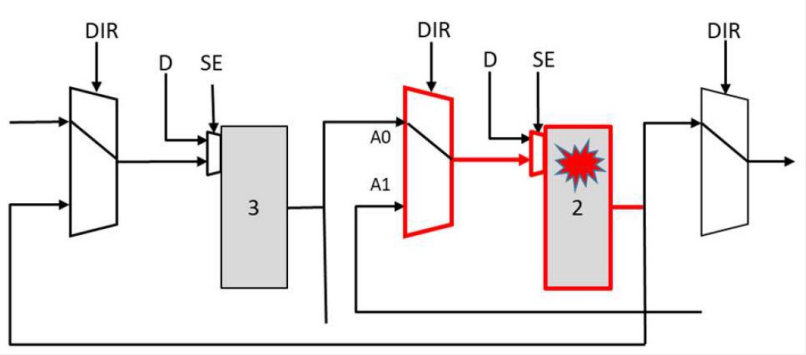


1. Load pattern from L2R: 111111
2. Unload pattern from R2L: 111000
3. Load pattern from R2L: 111111
4. Unload pattern from L2R: 000001

Reversible Scan Chain Diagnosis

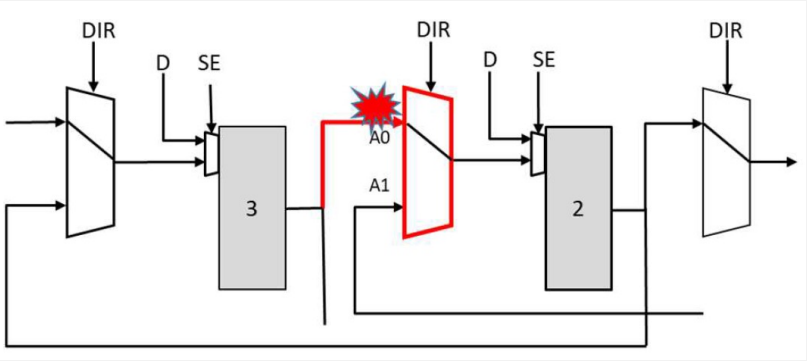
Dual-lane failure

- Patterns in both the directions fail
- Suspects: Direction mux, flop input and output



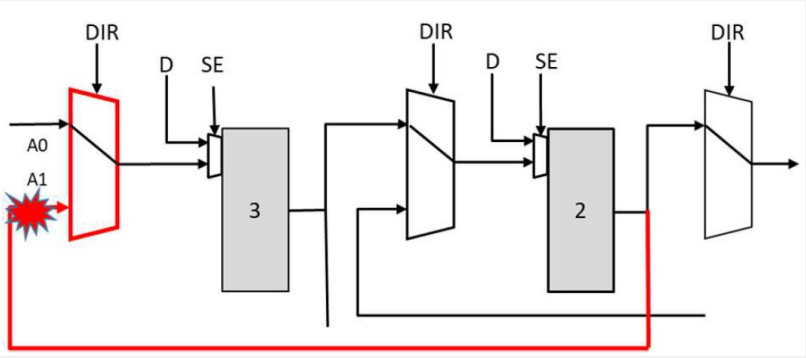
Left-to-right single-lane failure:

- Pattern in the forward direction fails
- Suspects: Direction mux and its A0 input

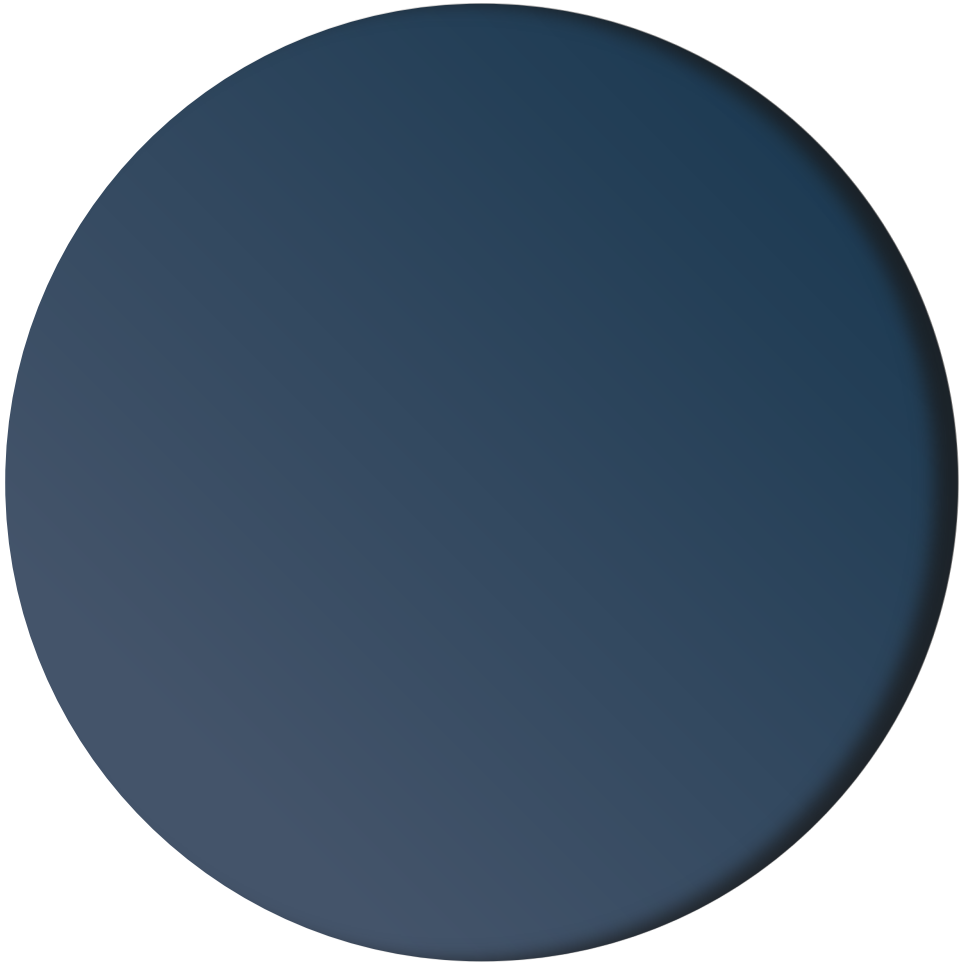


Right-to-left single-lane failure:

- Pattern in the reverse direction fails
- Suspects: Direction mux and its A1 input



Silicon Evaluation



Silicon Evaluation

Design overhead is 10-15% in terms of area and wirelength

Analysis of >1000 fails from multiple wafers of a test chip in a cutting-edge node:

1.5X

Failure Detection

More fails expected due to reverse path fails

4X

Diagnosis Runtime

Faster diagnosis because flush patterns are only used

Accurate

Failure Analysis

Confirmed diagnosis accuracy with FA

6X

Ideal Diagnostics

4X

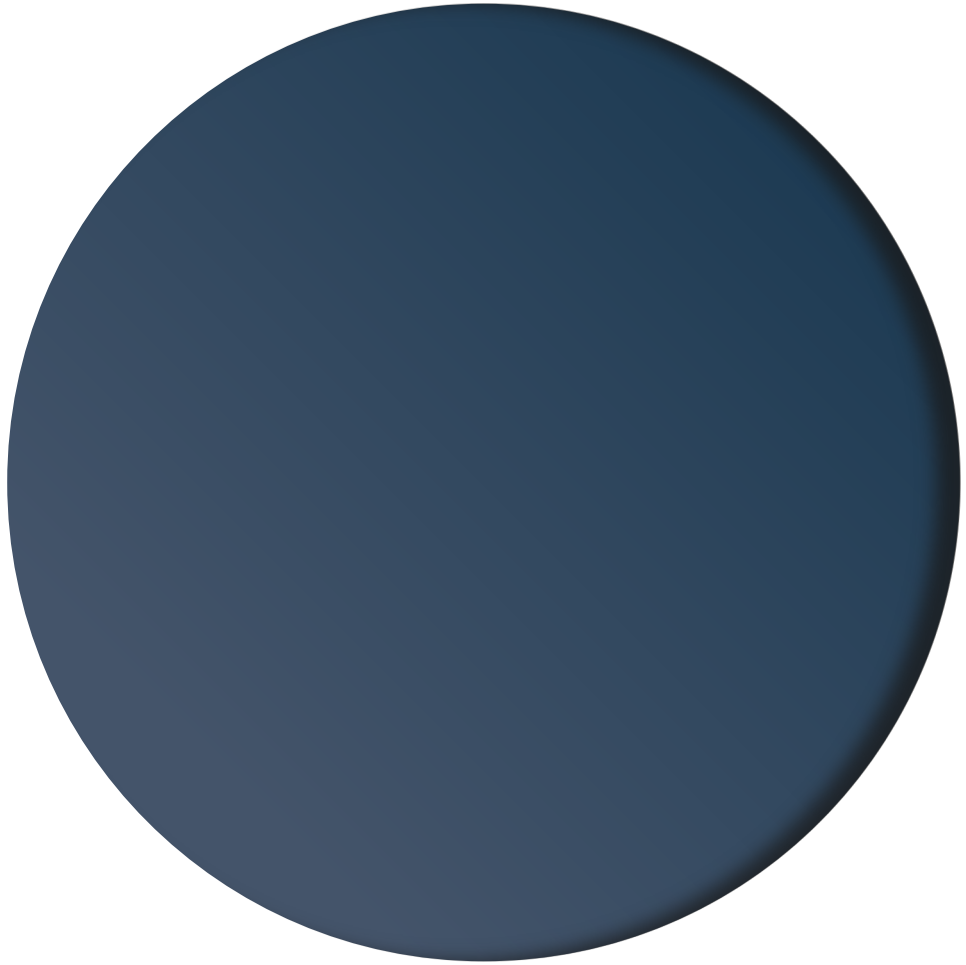
Logic Resolution

2X

Physical Area

Single-lane vs. dual lane differentiation increases number of single-suspect diagnostics, and reduces diagnostics noise and FA search space. Ideal multiple-defect diagnostics count improved 7X.

Failure Analysis



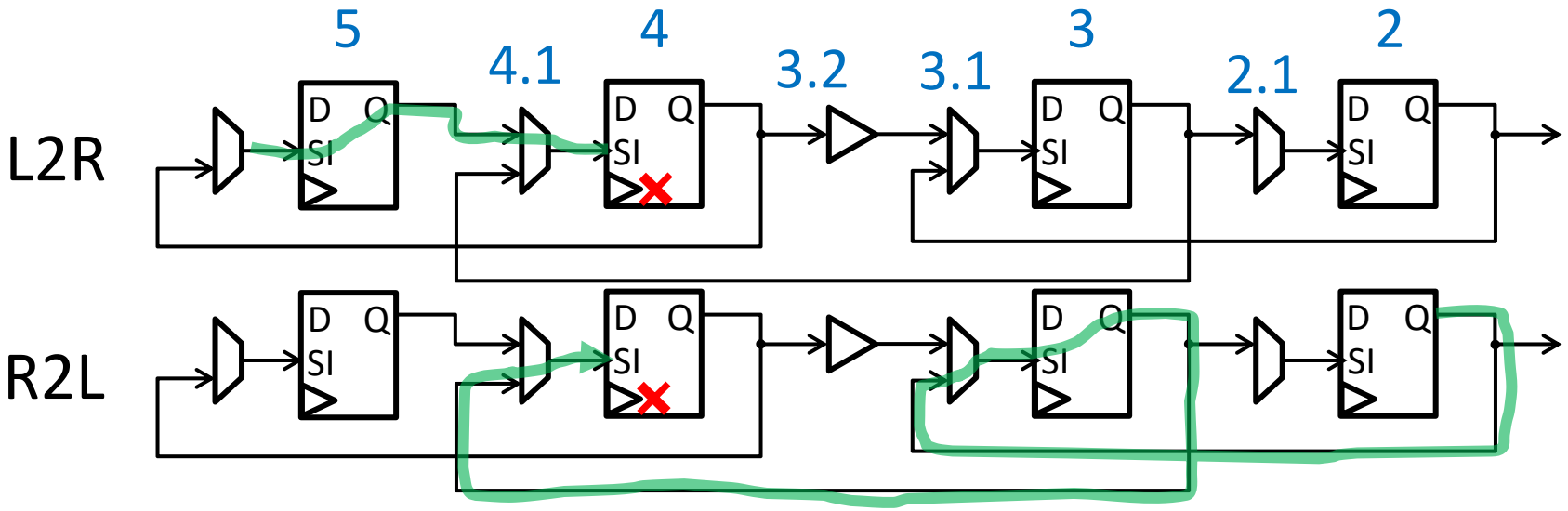
Case 1: Better Resolution (Dual-lane)

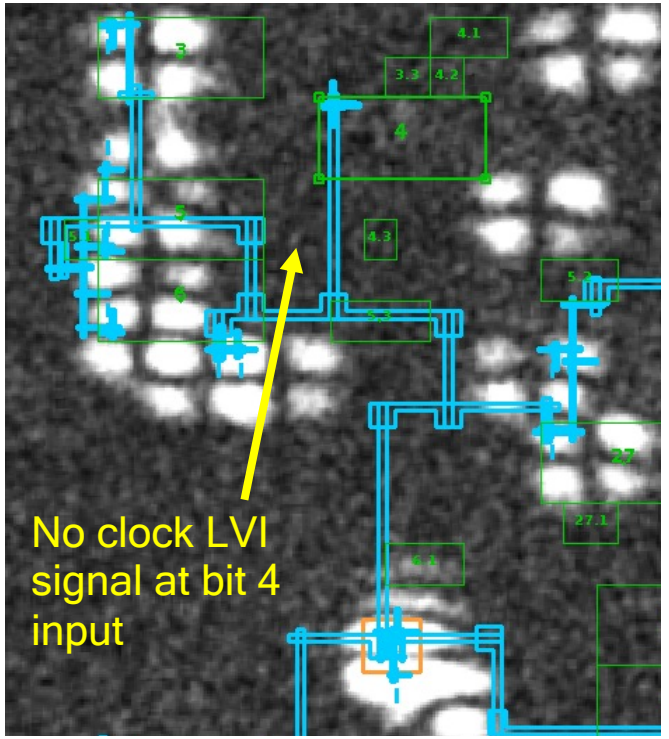
	Suspect cell	Laser Voltage Imaging (LVI)
Conventional	2.1 – 4.1	Discontinuity on the CLK signal path going to cell 4. CLK failure causes Q output of bit 4 to be stuck.
Reversible	3.1 – 4.1	

LVI confirms dual-lane defect in cell 4.

PFA: Defect found in transistor inside cell 4.

Conclusion: Reversible has better resolution & is accurate





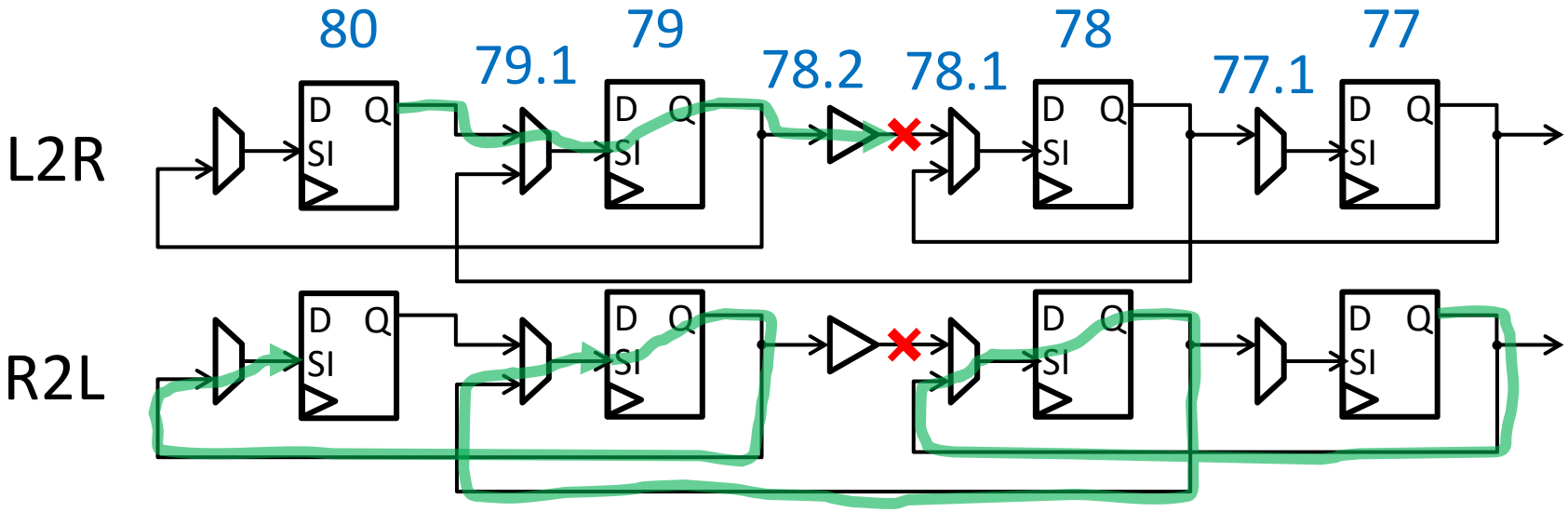
Case 2: Better Resolution (Single-lane)

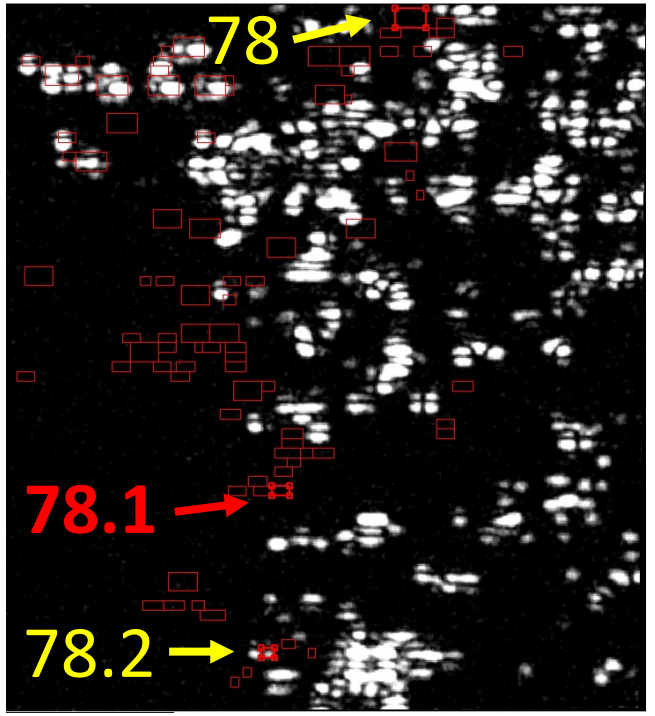
	Suspect cell	Laser Voltage Imaging (LVI)
Conventional	77.1 – 79.1	Data present up to 78.2, missing at 78.1 and 78
Reversible	78.1 – 79.1	R2L vector passing. Data present at 78.1 and 78

LVI confirms L2R single-lane defect between 78.2 and 78.1

PFA: Defect found in transistor connected to 78.1 input

Conclusion: Reversible has better resolution & is accurate



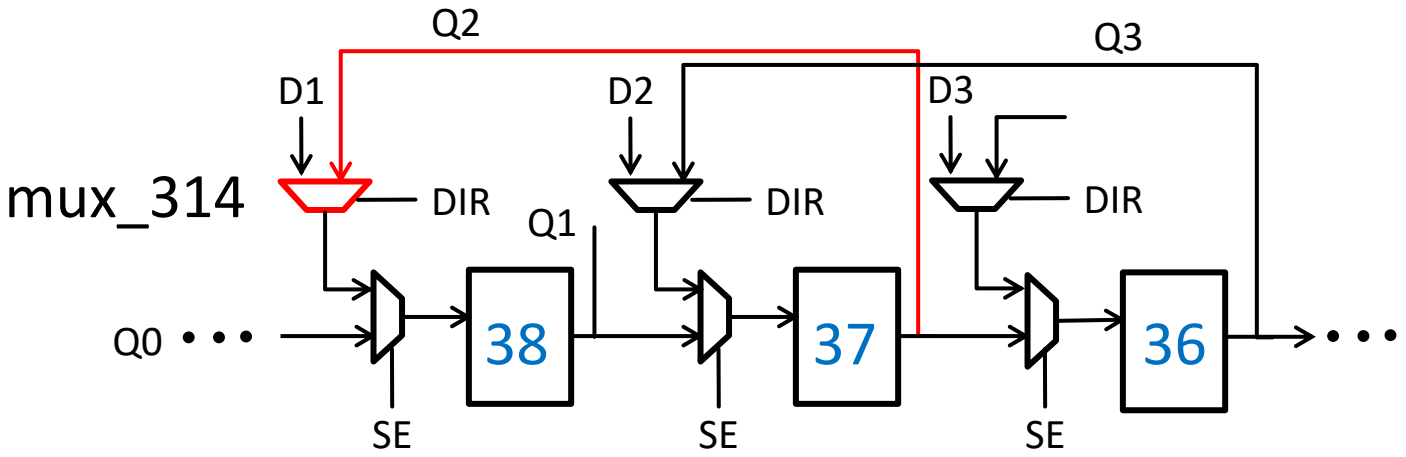


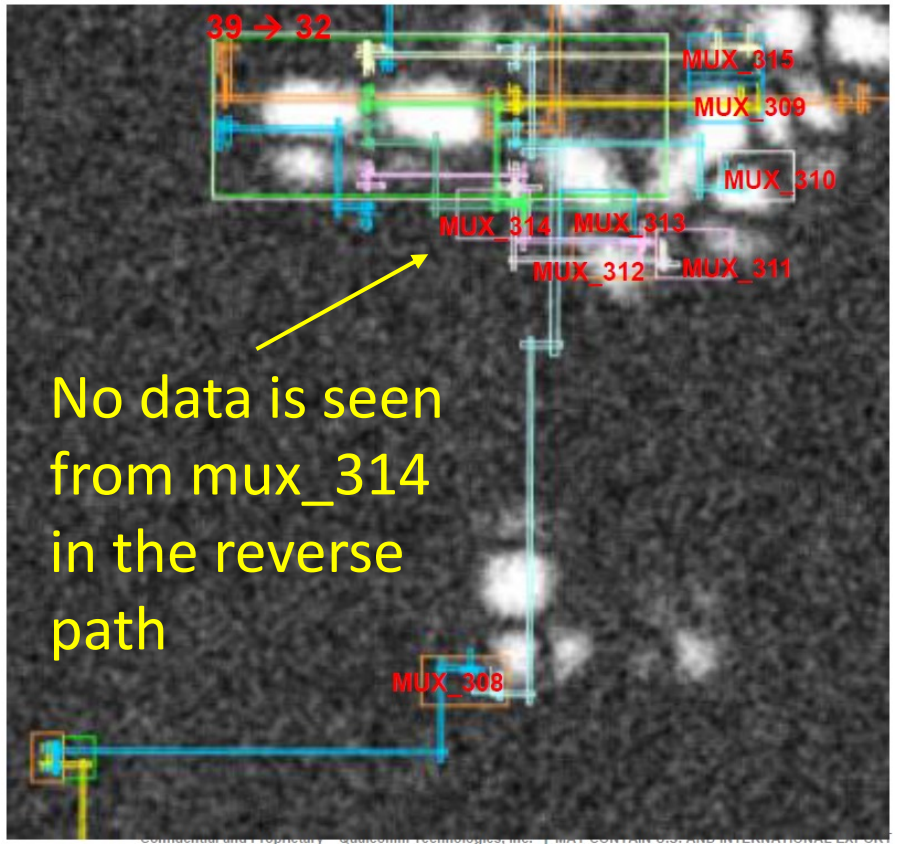
Case 3: Reversible Chain-only Fail (Single-lane)

	Suspect cell	Laser Voltage Imaging (LVI)
Conventional	-	L2R vector passing. Data present at position 37
Reversible	37	Discontinuity on mux_314 connected to Q2

LVI confirms R2L single-lane defect at mux_314 input connected to Q2

Conclusion: Reversible is accurate





Conclusion

- Reversible chain is a novel architecture that shifts data in two directions
- Chain and pattern bidirectionality enhances diagnosis
- Silicon evaluation shows 4X less runtime, 6X more perfect diagnoses, and 2X smaller search space for FA
- Optical and physical FA confirms diagnosis accuracy
- Future work is to find the right tradeoff between design cost, diagnostics quality and FA resources